CA-IF1044 Automotive CAN Transceiver with Standby Mode

1. Features

- **Meets the ISO 11898-2:2016 and ISO 11898-5:2007 physical layer standards**
- **Support classic CAN and 5 Mbps CAN FD**
- **Low-Current Standby Mode**
- **Ideal passive behavior when unpowered**
  - Bus and logic terminals are high impedance (no load)
  - Power up/down with glitch free operation on bus and RXD output
- **3.0V to 5.5V Logic-Supply (V_{IO}) Range**
- **Integrated protection increases robustness**
  - ±58V fault-tolerant CANH and CANL
  - ±30V extended common-mode input range (CMR)
  - Undervoltage protection on V_{CC} and V_{IO} supply terminals
  - Transmitter dominant timeout prevents lockup, data rates down to 4 kbps
  - Thermal shutdown protection (TSD)
- **Typical loop delay: 160ns**
- **–55°C to 150°C Junction Temperatures Range**
- **Available in SOIC8 and DFN8 packages**
- **AEC-Q100 Qualified and –40°C to 125°C Grade 1 operating temperature range**

2. Applications

- Body electronics
- Automotive gateway
- Advanced driver assistance systems (ADAS)
- Infotainment and cluster

3. General Description

The CA-IF1044x devices are control area network (CAN) transceivers with integrated protection for industrial and automotive applications. These devices are designed for using in CAN FD (flexible data rate) networks up to 5 Mbps data rate and feature ±58V extended fault protection on the CAN bus for equipment where overvoltage protection is required. This family of CAN transceivers also incorporate an input common-mode range(CMR) of ±30V, exceeding the ISO 11898 specification of -2V to +7V, well suited for applications where ground planes from different systems are shifting relative to each other.

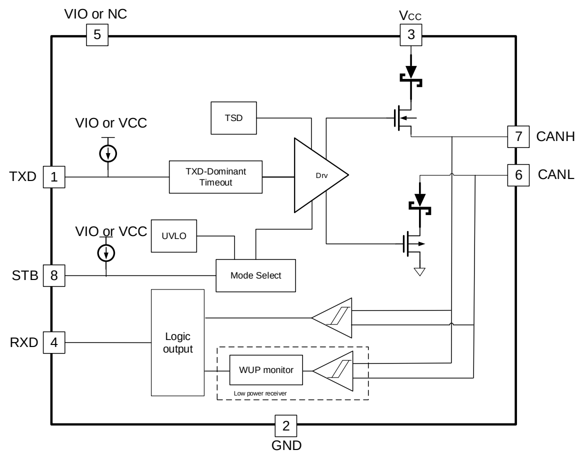
The CA-IF1044x series devices include a dominant timeout to prevent bus lockup caused by controller error or by a fault on the TXD input. When the TXD remains in the dominant state (low) for longer than t_{DOM}, the driver is switched to the recessive state, releasing the bus and allowing other nodes to communicate. The transceivers feature a STB pin for two modes of operation: normal high-speed mode and standby mode for low current consumption. Also, the CA-IF1044Vx devices in this family provide low level translation to simplify the interface with 5V, or 3.3V low voltage CAN controllers.

The CA-IF1044x family of devices is available in a standard 8-pin narrow-body SOIC package and small size 8-pin DFN package, operates over the -55°C to +150°C junction temperature range. AEC-Q100 qualified for automotive applications.

Table 3-1. Device Information

Part number	Package	Package size(NOM)
CA-IF1044S-Q1	SOIC8	4.9mm x 3.9mm
CA-IF1044VS-Q1	SOIC8	4.9mm x 3.9mm
CA-IF1044D-Q1	DFN8	3.0mm x 3.0mm
CA-IF1044VD-Q1	DFN8	3.0mm x 3.0mm

Simplified Block Diagram



4. Ordering Information

Table 4-1. Ordering Information

Part Number	Features	Package
CA-IF1044S-Q1	Pin 5 = NC	SOIC8
CA-IF1044VS-Q1	With low level translation, Pin 5 = V_{IO}	SOIC8
CA-IF1044D-Q1	Pin 5 = NC	DFN8
CA-IF1044VD-Q1	With low level translation, Pin 5 = V_{IO}	DFN8

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5. Revision History

Revision Number	Description	Page Changed
Version 1.00	N/A	N/A
Version 1.01	Typo error	6
Version 1.02	Update the V_{uv_vcc} and I_{LKG} spec.	6,7
Version 1.03	Update the V_{IO} Logic Supply Voltage Range	5
Version 1.04	Update Tape and Reel Information	23

6. Pin Configuration and Functions

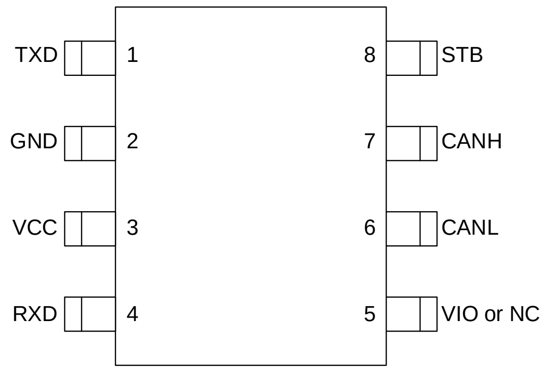


Figure 6-1. CA-IF1044x Pin Configuration

Table 6-1. CA-IF1044x Pin Configuration and Description

Pin #		Pin Name	Type	Description
CA-IF1044S-Q1 CA-IF1044D-Q1	CA-IF1044VS-Q1 CA-IF1044VD-Q1			
1	1	TXD	Digital I/O	Transmit Data Input, Drive TXD high to set the driver in the recessive state. Drive TXD low to set the driver in the dominant state. TXD is a CMOS/TTL compatible input from a CAN controller with an internal pull-up to V_{CC} or V_{IO}.
2	2	GND	GND	Ground.
3	3	V_{CC}	Power	+5V Supply Voltage. Bypass V_{CC} to GND with an at least 0.1µF capacitor.
4	4	RXD	Digital I/O	Receive Data Output, RXD is LOW for dominant bus state and HIGH for recessive bus state. RXD is a CMOS/TTL compatible output from the physical bus lines CANH and CANL.
5	-	NC	NC	No connect.
-	5	V_{IO}	Power	Logic Supply Input. V_{IO} is the logic supply voltage for the input/output between the CAN transceiver and controller. V_{IO} allows full compatibility from +1.8V to +5.5V logic on all digital lines. Bypass to GND with a 0.1µF capacitor. Connect V_{IO} to V_{CC} for 5V logic compatibility.
6	6	CANL	Bus I/O	CAN bus line low.
7	7	CANH	Bus I/O	CAN bus line high.
8	8	STB	Digital I/O	Standby Mode. A logic-high on STB pin or leave it open to select the standby mode. In standby mode, the transceiver is not able to transmit data and the receiver is in low-power mode. A logic-low on STB pin puts the transceiver in normal operating mode.

7. Specifications

7.1. Absolute Maximum Ratings

PARAMETER		MIN	MAX	UNIT
V_{CC}	5V Bus Supply Voltage Range	-0.3	7	V
V_{IO}	Logic Supply Voltage Range	-0.3	7	V
V_{BUS}	CAN Bus I/O voltage range (CANH,CANL)	-70	70	V
$V_{(DIFF)}$	Max differential voltage between CANH and CANL	-70	70	V
$V_{(Logic\_Input)}$	Logic input terminal voltage range (TXD, S)	-0.3	+7	V
$V_{(Logic\_Output)}$	Logic output terminal voltage range (RXD)	-0.3	+7	V
$I_{O(RXD)}$	RXD (receiver) terminal output current	-8	8	mA
T_J	Virtual junction temperature range	-55	150	℃
T_{STG}	Storage temperature range	-65	150	℃

Note:

1. The stresses listed under “Absolute Maximum Ratings” are stress ratings only, not for functional operation condition. Exposure to absolute maximum rating conditions for extended periods may cause permanent damage to the device.

7.2. ESD Ratings

Parameters	TEST CONDITIONS		VALUE	UNIT
CA-IF1044S				
HBM[1] ESD	CAN bus terminals (CANH, CANL) to GND, per AEC-Q100-002[1] HBM ESD protection classification level 3B		±8000	V
	Other pins, per AEC-Q100-002[1] HBM ESD protection classification level 3A		±6000	
CDM ESD	All pins		±2000	V
System Level ESD	CAN bus terminals (CANH, CANL) to GND	IEC 61000-4-2: unpowered contact discharge.	±6000[2]	V

Note:

1. Per AEC Q100-002, HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.
2. Testing on System Board Level.

7.3. Recommended Operating Conditions

PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage Range	4.5		5.5	V
V_{IO}	Logic Supply Voltage Range	3.0		5.5	V
$I_{OH(RXD)}$	RXD terminal high level output current	-2			mA
$I_{OL(RXD)}$	RXD terminal low level output current			2	mA

7.4. Thermal Information

Thermal Metric		DFN8	SOIC8	UNIT
$R_{\theta JA}$	Junction to Ambient	40	170	°C/W

7.5. Electrical Characteristics

Over recommended operating conditions, T_A = –40°C to 125°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER						
I_{CC}	5V Supply Current	TXD=0V, STB=0V, R_L = 60 Ω (dominant) see Figure 8-1		45	70	mA
		TXD=0V, STB=0V, RL=50 Ohm (dominant) see Figure 8-1		50	80	mA
		TXD=0V, STB=0V, CANH=-12V (dominant) see Figure 8-1			130	mA
		TXD=V_{CC} or V_{IO}, STB=0V, RL=50 Ohm (recessive) see Figure 8-1		4.5	7.5	mA
		TXD = STB = V_{IO}(standby, CA-IF1044Vx), RL = 50 Ohm see Figure 8-1		0.5	3	µA
		TXD = STB = V_{CC} (standby, CA-IF1044S-Q1/CA-IF1044D-Q1), RL = 50 Ohm, see Figure 8-1		22	35	µA
I_{IO}	I/O Supply Current	TXD = 0V, STB = 0V, RXD open (CA-IF1044Vx)		125	300	µA
		TXD= V_{IO}, STB= V_{IO}, RXD open (CA-IF1044Vx)		70	150	µA
I_{IO}	I/O Supply Current (standby)	TXD= STB= V_{IO}, RXD open (CA-IF1044Vx)		20	33	µA
V_{uv_vcc}	V_{CC} UVLO Threshold	Rising		4.2	4.45	V
V_{uv_vcc}	V_{CC} UVLO Threshold	Falling	3.65	4.0	4.4	V
$V_{uv\_vcc\_sd}$	V_{CC} UVLO Shutdown Threshold	Rising		1.56	1.9	V
$V_{uv\_vcc\_sd}$	V_{CC} UVLO Shutdown Threshold	Falling	1.3	1.51	1.85	V
V_{UV_VIO}	UVLO threshold on V_{IO}	Rising (CA-IF1044Vx)		1.56	1.9	V
V_{UV_VIO}	UVLO threshold on V_{IO}	Falling (CA-IF1044Vx)	1.3	1.51	1.85	V
LOGIC INTERFACE (Mode select input, STB)						
V_{IH}	High-level input voltage		0.7xV_{IO}			V
V_{IL}	Low-level input voltage				0.3xV_{Io}	V
I_{IH}	High-level input leakage current	STB = V_{CC} = V_{IO} = 5.5V	-2		2	µA
I_{IL}	Low-level input leakage current	STB = 0V, V_{CC} = V_{IO} = 5.5V	-200	-100	-20	µA
$I_{lek(off)}$	Unpowered leakage current	STB=5.5V, V_{CC} = V_{IO} = 0V	-1		1	µA
LOGIC INTERFACE (CAN transmit data input, TXD)						
V_{IH}	High-level input voltage		0.7xV_{Io}			V
V_{IL}	Low-level input voltage				0.3xV_{Io}	V
I_{IH}	High-level input leakage current	TXD = V_{CC} = V_{IO} = 5.5V	-2.5	0	1	µA
I_{IL}	Low-level input leakage current	TXD = 0V, V_{CC} = V_{IO} = 5.5V	-200	-100	-20	µA
$I_{lek(off)}$	Unpowered leakage current	TXD = 5.5V, V_{CC} = V_{IO} = 0V	-1	0	1	µA
C_i	Input capacitance	V_{IN} = 0.4*sin(4E6*π*t) + 2.5V		5		pF
LOGIC INTERFACE (CAN receive data output, RXD)						
V_{OH}	High-level output voltage	Io = -2mA, see Figure 8-2	0.8xV_{Io}			V
V_{OL}	Low-level output voltage	Io = +2mA, V_{IO}=2.5V- 5.5V, see Figure 8-2			0.2xV_{Io}	V
		Io = +2mA, V_{IO}=1.8V-2.5V, see Figure 8-2			0.25xV_{Io}	V
$I_{lek(off)}$	Unpowered leakage current	STB = 5.5V, V_{CC} = 0V, V_{IO}=0V	-1	0	1	µA
Devices						
T_{TSD}	Thermal shutdown temperature			190		°C
T_{TSD_HYS}	Thermal shutdown temperature threshold hysteresis			10		°C
CAN BUS DRIVER						
$V_{O(DOM)}$	Bus output voltage (dominant)	TXD = low, STB = 0V, R_L=50 -65 Ω, CL=open, RCM=open, CANH, see Figure 8-1	2.75		4.5	V
		TXD = low, STB = 0V, R_L = 50 -65 Ω, CL=open, RCM=open, CANL, see Figure 8-1	0.5		2.25	V

Electrical Characteristics (continued)

Over recommended operating conditions, T_A = –40°C to 125°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CAN BUS DRIVER						
$V_{OD(DOM)}$	Bus output differential voltage (dominant)	TXD = low, STB=0V, RL=45-50 Ohm, RCM open, see Figure 8-1	1.4		3.3	V
		TXD = low, STB=0V, RL=50-65 Ohm, RCM open, see Figure 8-1	1.5		3.0	V
		TXD = low, STB = 0V, RL=2240 Ohm, RCM open, see Figure 8-1	1.5		5.0	V
$V_{O(REC)}$	Bus output voltage (recessive)	TXD=V_{CC} or V_{IO}， V_{CC} = $V_{IO,}$ STB=0V, RL=open, RCM=open, CANH,CANL, see Figure 8-1	2		3	V
$V_{OD(REC)}$	Bus output differential voltage (recessive)	TXD = high, STB=0V, R_L=60 Ω, CL=open, RCM=open, see Figure 8-1	-120		12	mV
		TXD = high, STB=0V, no load, CL=open, RCM=open, see Figure 8-1	-50		50	mV
$V_{O(STB)}$	Bus output at standby mode	STB=V_{IO}, RL open, RCM open, CANH	-0.1		0.1	V
		STB= V_{IO}, RL open, RCM open, CANL	-0.1		0.1	V
		STB= V_{IO}, RL open, RCM open, CANH-CANL	-0.2		0.2	V
$I_{OS(SS\_DOM)}$	Short-circuit current (dominant)	TXD = low, STB=0V, CANL open, V_{CANH}= -5V to 40V, see Figure 8-7	-115			mA
		TXD = low, STB=0V, CANH open, V_{CANL} = -5V to 40V, see Figure 8-7			115	
$I_{OS(SS\_rec)}$	Short-circuit current (recessive)	TXD = high, STB=0V ,V_{BSU} = CANH = CANL = -27V to 32V, see Figure 8-7	-6		6	mA
V_{SYM}	Transient symmetry (dominant or recessive)	R_L = 60 Ω, STB=0V, R_{CM} open, C_{split}=4.7nF, RCM open , TXD = 250kHz, 1MHz, 2.5M Hz, see Figure 8-1	0.9		1.1	V/V
V_{SYM_DC}	DC Output symmetry (dominant or recessive)	RL =60 Ω, STB = 0, R_{CM} open, see Figure 8-1	-0.4		0.4	V
CAN RECEIVER						
V_{CM}	Common-mode input range	CANH or CANL to GND, RXD output valid, see Figure	-30		+30	V
		Standby mode, V_{IO}>2.5V, RXD output valid, see Figure	-20		20	
		Standby mode, V_{IO} ≤2.5V, RXD output valid, see Figure	-12		12	
V_{IT}	Input differential threshold voltage at normal mode	STB = 0V, V_{CM} from -20V to 20V, see Figure 8-2	500		900	mV
		STB=0V, V_{CM} from -30V to 30V, see Figure 8-2	400		1000	mV
$V_{IT(STB)}$	Input differential threshold at standby mode	STB = high, see Figure	400		1150	mV
V_{DIFF_D}	Input differential threshold voltage at normal mode (dominant)	STB=0V, V_{CM} from -20V to 20V, see Figure 8-2	0.9		9	V
		STB=0V, V_{CM} from -30V to 30V, see Figure 8-2	1		9	
V_{DIFF_R}	Input differential threshold voltage at normal mode (recessive)	STB=0V, V_{CM} from -20V to 20V, see Figure 8-2	-4		0.5	V
		STB=0V, V_{CM} from -30V to 30V, see Figure 8-2	-4		0.4	
$V_{DIFF\_D(STB)}$	Input differential threshold voltage at standby mode (dominant)	STB=high, see Figure 8-2	1.15		9	V
$V_{DIFF\_R(STB)}$	Input differential threshold voltage at standby mode (recessive)	STB=high, see Figure 8-2	-4		0.4	V
$V_{DIFF\_(HYST)}$	Input differential threshold hysteresis	normal mode		100		mV
R_{IN}	CANH/CANL input resistance	TXD = high, STB = 0, V_{CM} = -30V to 30V	20		45	kΩ
R_{DIFF}	Differential input resistance	TXD = high, STB = 0, V_{CM} = -30V to 30V	40		90	kΩ
$R_{DIFF\ (M)}$	Input resistance matching	V_{CANH} = V_{CANL} =5V	-1		1	%
I_{LKG}	Input Leakage Current	V_{IO} = V_{CC} = 0V, V_{CANH} = V_{CANL} =5V			8	μA
C_{IN}	Input capacitance	CANH or CANL to GND, TXD=V_{CC}, V_{IO} = V_{CC}, STB = 0		20		pF
C_{IN_DIFF}	Differential input capacitance	CANH to CANL, TXD = High		10		pF

7.6. Switching Characteristics

Over recommended operating conditions, T_A = –40°C to 125°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DRIVER						
t_R	Differential output rise time	STB=0V, R_L=60Ω, C_L=100pF , see Figure 8-1		30		ns
t_F	Differential output fall time	STB=0V, R_L=60Ω, C_L=100pF, see Figure 8-1		50		ns
t_{ONTXD}	TXD propagation delay (recessive to dominant)	STB = 0, R_L=60Ω, C_L=100pF, see Figure 8-1		80		ns
t_{OFFTXD}	TXD propagation delay (dominant to recessive)	STB = 0, R_L=60Ω, C_L=100pF, see Figure 8-1		70		ns
Tsk(p)	Pulse skew	STB=0V, R_L=60Ω, C_L=100pF, see Figure 8-1		20		ns
t_{DOM}	TXD-dominant Timeout	R_L=60 Ω, C_L open, see Figure 8-5	2	5	8	ms
RECEIVER						
t_{ONRXD}	RXD propagation delay (recessive to dominant)	STB = 0, C_{RXD}=15pF, see Figure		65		ns
t_{OFFRXD}	RXD Propagation delay (dominant to recessive)	STB = 0, C_{RXD} =15pF, see Figure		90		ns
t_R	Receiver output rise time	STB=0 V , C_{RXD} =15pF, see Figure		10		ns
t_F	Receiver output fall time	STB=0 V , C_{RXD} =15pF, see Figure		10		ns
DEVICE						
t_{loop1}	Total loop delay, driver input (TXD) to receiver output (RXD), recessive to dominant	R_L=60Ω, C_L=100pF, see Figure 8-3		125	210	ns
t_{loop2}	Total loop delay, driver input (TXD) to receiver output (RXD), dominant to recessive	R_L=60Ω, C_L=100pF, see Figure 8-3		150	210	ns
t_{MODE}	Mode change time, from normal to standby or from standby to normal	see Figure 8-4			20	µs
T_{wk_FILTER}	Filter time for a valid wake-up pattern	see Figure 8-4	0.5		1.8	µs
$T_{WK\_FILTEROUT}$	Bus wake-up timeout	see Figure 8-4	0.8		6	ms
FD TIMING						
$t_{bit(bus)}$	Bit time on CAN bus output pins with $t_{BIT(TXD)}$ = 500 ns	STB = 0, R_L=60Ω, C_L=100pF, C_{RXD} =15pF, see Figure 8-6	450		530	ns
$t_{bit(bus)}$	Bit time on CAN bus output pins with $t_{BIT(TXD)}$ = 200 ns	STB = 0, R_L=60Ω, C_L=100pF, C_{RXD} =15pF, see Figure 8-6	155		210	ns
$t_{bit(rxd)}$	Bit time on RXD output pins with $t_{BIT(TXD)}$ = 500 ns	STB = 0, R_L=60Ω, C_L=100pF, C_{RXD} =15pF, see Figure 8-6	400		550	ns
$t_{bit(rxd)}$	Bit time on RXD output pins with $t_{BIT(TXD)}$ = 200 ns	STB = 0, R_L=60Ω, C_L=100pF, C_{RXD} =15pF, see Figure 8-6	120		220	ns
t_{rec}	Receiver timing symmetry with $t_{BIT(TXD)}$ = 500ns	STB = 0, R_L=60Ω, C_L=100pF, C_{RXD} =15pF, see Figure 8-6	-50		20	ns
t_{rec}	Receiver timing symmetry with $t_{BIT(TXD)}$ = 200ns	STB = 0, R_L=60Ω, C_L=100pF, C_{RXD} =15pF, see Figure 8-6	-45		15	ns

8. Parameter Measurement Information

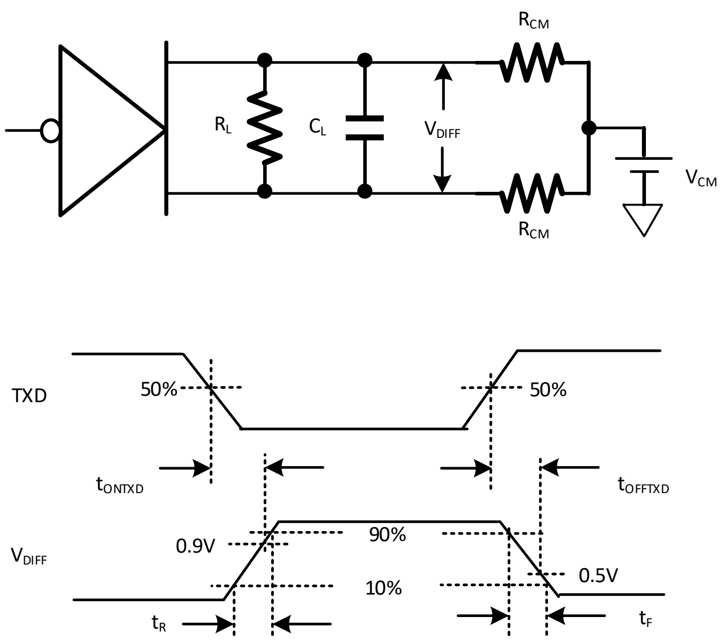


Figure 8-1. Transmitter Test Circuit and Timing Diagram

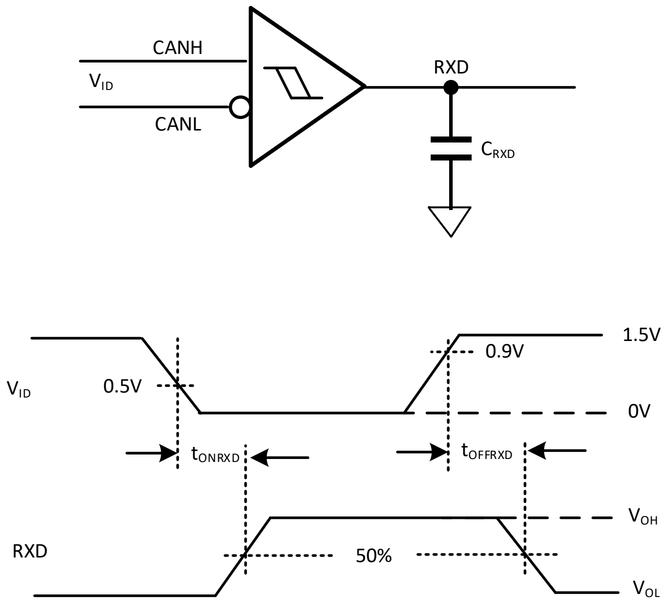


Figure 8-2. Receiver Test Circuit and Measurement

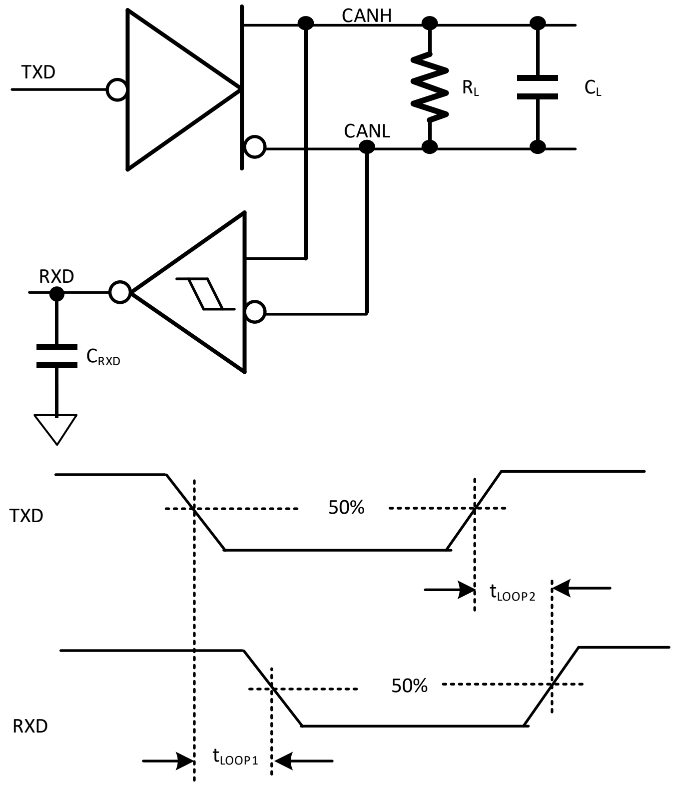


Figure 8-3. TXD to RXD Loop Delay

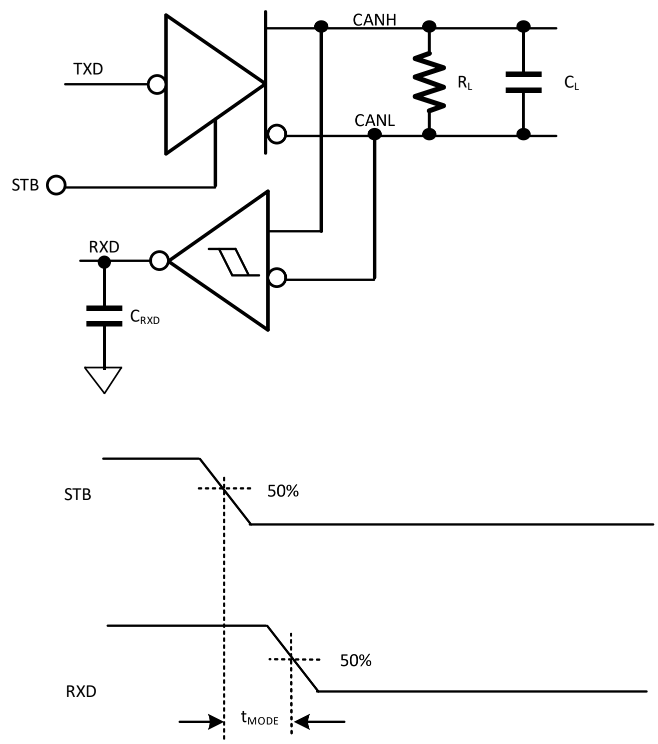


Figure 8-4. Mode Change Test Circuit and Measurement

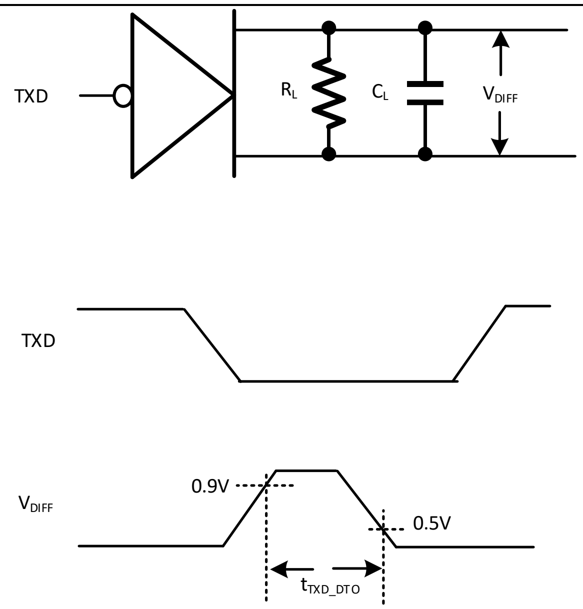


Figure 8-5. Transmitting Dominant Timeout Timing Diagram

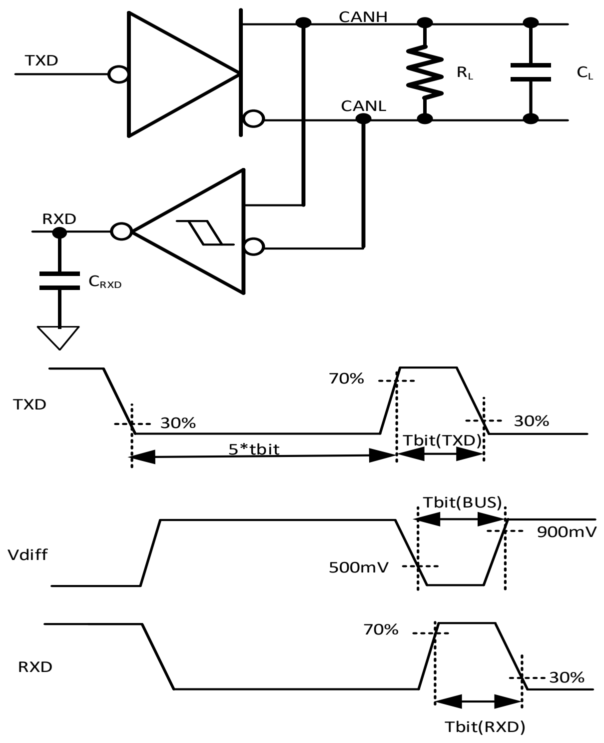


Figure 8-6. CAN FD Timing Parameter Measurement

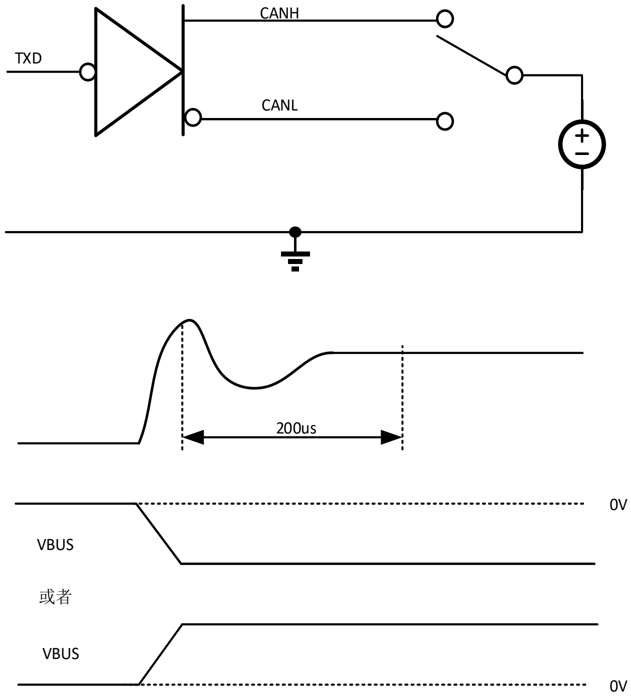


Figure 8-7. Driver Short Circuit Current Test Circuit and Measurement

9. Detailed Description

The CA-IF1044x family of devices is fault-protected Controller Area Network (CAN) transceiver, meets the ISO11898-2 (2016) high speed CAN physical layer standard. These devices are designed for harsh industrial and automotive applications with a number of integrated robust protection features set that improve the reliability of end equipment. All devices are fault protected up to ±58V for the bus pins, making them ideal for applications where overvoltage protection is required. A common-mode voltage range of ±30V enables communication in noisy environments where there are ground plane differences between different systems. Dominant timeout prevents the bus from being blocked by a hung-up microcontroller, and the outputs CANH and CANL are short-circuit current-limited and protected against excessive power dissipation by thermal shutdown circuitry that places the driver outputs in a high-impedance state.

A separate input V_{IO} allows the CA-IF1044Vx devices to communicate with logic systems down to 3.3V while operating up to a +5V bus supply. This provides a reduced input voltage threshold to the TXD and STB inputs, and provides a logic-high output at RXD compatible with the microcontroller's supply rail. The logic compatibility eliminates external logic level translator and longer propagation delay due to level shifting. Connect V_{IO} to V_{CC} to operate with +5V logic systems.

The CA-IF1044x devices can operate up to 5Mbps data rate and support CAN FD. However, the maximum data rate is limited by the bus loading, number of nodes, cable length etc. factors, for CAN network design, margin must be given for signal loss across the system and cabling, parasitic loadings, timing, network imbalances, ground offsets and signal integrity thus a practical maximum data rate, number of nodes often lower than the theoretical value.

9.1. CAN Bus Status

The CAN bus has two states: dominant and recessive. In the dominant state (a zero bit, used to determine message priority), CANH-CANL are defined to be logic ‘0’ when the voltage across them is between +1.5V and +3V (higher than 0.9V). In the recessive state (a 1-bit and the state of the idle bus), the driver is defined to be logic ‘1’ when differential voltage is between -120mV and +12mV, or when it is near zero(lower than 0.5V), see Figure 9-1 for the bus logic state voltage definition.

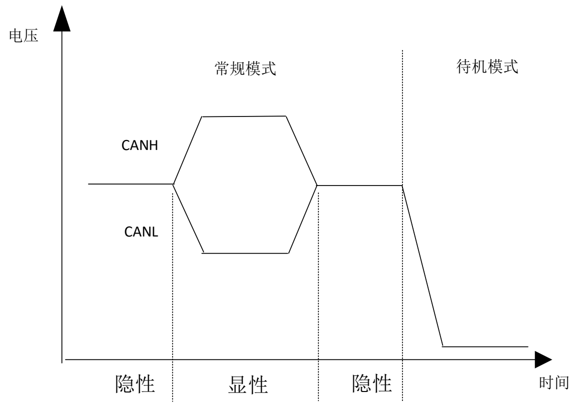


Figure 9-1. Bus Logic State Voltage Definition

9.2. Receiver

The receiver of CA-IF1044x family of devices includes a main receiver to support normal bi-directional communication and a low-power receive channel to monitor the bus line and detect the wakeup event on the bus line during standby mode. In normal operation (STB = low), the main receiver reads the differential input from the bus line (CANH and CANL) and transfers this data as a single-ended output RXD to the CAN controller. The internal comparator senses the difference voltage V_{DIFF} = (V_{CANH}-V_{CANL}), with respect to an internal threshold of 0.7V. If V_{DIFF} > 0.9V, a logic-low is present on RXD; If V_{DIFF} < 0.5V, a logic-high is present. The CANH and CANL common-mode range is ±30V in normal mode. See Figure 9-2 for the receiver input bias circuit.

Drive the STB pin high or leave it open for operating at standby mode, in this case, the main receiver is disabled and the low-power receive channel is enabled. This switches the receiver to a low current and low-speed state. The bus line is monitored by a low-power differential comparator to detect and recognize a wakeup event on the bus line. RXD is logic High until a valid wake-up is received. Once a valid remote wake-up event occurred, RXD transition to logic Low.

RXD is a logic-high when CANH and CANL are shorted or terminated and un-driven in both normal mode and standby mode, see Table 9-1 for more details about the receiver truth table.

Table 9-1. Receiver Truth Table

DEVICE MODE	$V_{ID} = V_{CANH}-V_{CANL}$	BUS STATE	RXD
Normal STB = Low	$V_{ID} \geq 0.9V$	Dominant	Low
	$0.5V < V_{ID} < 0.9V$	Indeterminate	Indeterminate
	$V_{ID} \leq 0.5V$	Recessive	High
Standby STB = High or open	$V_{ID} > 1.15V$	Dominant	Low if a remote wake event occurred, otherwise output High.
	$0.4V < V_{ID} < 1.15V$	Indeterminate	Indeterminate
	$V_{ID} \leq 0.4V$	Recessive	High
Any	Open ($V_{ID} \approx 0V$)	Open	High

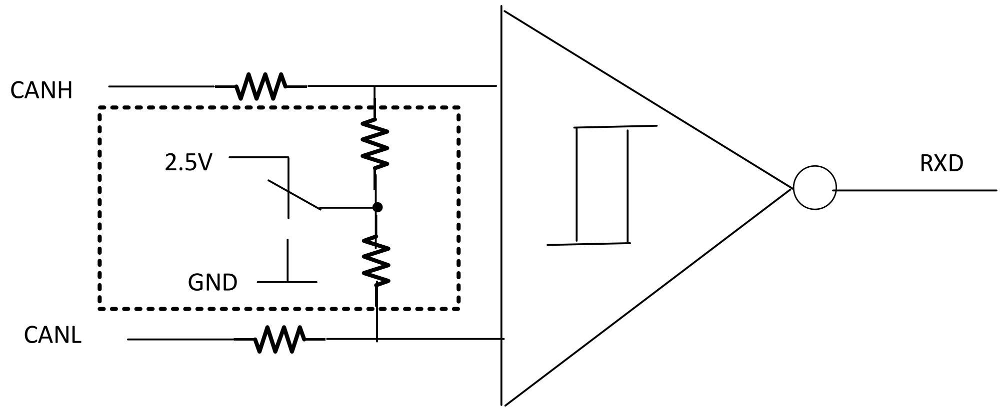


Figure 9-2. Receiver Input/Transmitter Output Bias Circuit

9.3. Transmitter

In normal operation (STB = Low), the transmitter converts a single-ended input signal (TXD) from the local CAN controller to differential outputs for the bus lines CANH and CANL. The truth table for the transmitter is provided in Table 9-2. The CA-IF1044x family of devices protects the transmitter output stage against a short-circuit to a positive or negative voltage by limiting the driver current. Thermal shutdown further protects the devices from excessive temperatures that may result from a short circuit. The transmitter returns to normal operation once the short is removed and the junction temperature drops at least the thermal shutdown hysteresis temperature below the thermal shutdown temperature of the device.

Drive the STB pin high for standby mode, the transmitter is disabled and put the bus in high-impedance with internal weak pull-down to ground, see Figure 9-2.

Table 9-2. Transmitter Truth Table (When Not Connected to the Bus)

INPUT		TXD LOW TIME	OUTPUT		BUS STATE
STB	TXD		CANH	CANL	
Low	Low	< t_{DOM}	High	Low	Dominant
	Low	> t_{DOM}	$V_{CC}/2$	$V_{CC}/2$	Recessive
	High or Open	X	$V_{CC}/2$	$V_{CC}/2$	Recessive
High or Open	X	X	High-Z	High-Z	Weak pull-down to GND

Note: X = Don't care, High-Z = High impedance.

9.4. Protection Functions

9.4.1. Undervoltage Lockout

Both the CA-IF1044S-Q1/CA-IF1044D-Q1 and the CA-IF1044Vx family of devices have undervoltage detection on V_{CC} supply terminal. For CA-IF1044S-Q1/CA-IF1044D-Q1, when the supply voltage V_{CC} is less than V_{UN_VCC} and greater than Vuv_vcc_sd, if STB = high, will put the device into low-power standby mode; if STB = low, will put the device into shutdown mode. If the supply voltage V_{CC} is less than Vuv_vcc_sd, will put the device into shutdown and disable both receiver and driver, leave the bus in high-impedance. See Table 9-3 for more details.

Table 9-3. CA-IF1044S-Q1/CA-IF1044D-Q1 Undervoltage Lockout

V_{CC}	DEVICE STATE	BUS OUTPUT	RXD
> V_{UV_VCC}	Normal	Per TXD	Mirrors Bus
V_{UV_VCC} > V_{CC} > Vuv_vcc_sd	Standby (STB = high)	Weak pull-down to GND	High until valid wake-up is received
	Shutdown mode (STB = low)	High-Z	High
< Vuv_vcc_sd	Shutdown mode	High-Z	High-Z

The CA-IF1044Vx devices also feature undervoltage detection on V_{IO} supply terminal, if the supply voltage V_{IO} is less than V_{UV_VIO}, will disable both receiver and driver, put the device into shutdown mode. When V_{IO} is in valid level but V_{CC} is less than V_{UN_VCC}, if STB = high, will place the device into low-power standby mode; if STB = low, will put the device into shutdown mode. See Table 9-4 for the undervoltage lockout status of CA-IF1044Vx.

Table 9-4. CA-IF1044Vx Undervoltage Lockout

V_{CC}	V_{IO}	DEVICE STATE	BUS OUTPUT	RXD
> V_{UV_VCC}	> V_{UV_IO}	Normal	Per TXD	Mirrors Bus
< V_{UV_VCC}	> V_{UV_IO}	Standby (STB = high)	Weak pull-down to GND	High until valid wake-up is received
		Shutdown mode (STB = low)	High-Z	High
> V_{UV_VCC}	< V_{UV_IO}	Shutdown mode	High-Z	High-Z
< V_{UV_VCC}	< V_{UV_IO}	Shutdown mode	High-Z	High-Z

Once the undervoltage condition is cleared and the supply voltage has returned to a valid level, the devices transition to normal mode after the t_{MODE} time has expired. The host controller should not attempt to send or receive messages until the t_{MODE} time has expired.

9.4.2. Fault Protection

The CA-IF1044x devices has an internal ±58V overvoltage protection circuit on the driver output and receiver input to protect the devices from accidental shorts between a local power supply and the data lines of the transceivers. This level of protection is present whether the transceiver is powered or un-powered.

9.4.3. Thermal Shutdown

If the junction temperature of the devices exceed the thermal shutdown threshold T_{TSD} (190°C), the device turns off the CAN driver circuits thus blocking the TXD-to-bus transmission path. The CAN bus terminals are biased to the recessive level during a thermal shutdown, and the receiver-to-RXD path remains operational. The shutdown condition is cleared when the junction temperature drops at least the thermal shutdown hysteresis temperature below the thermal shutdown threshold.

9.4.4. Current-Limit

The CA-IF1044x protect the transmitter output stage against a short-circuit to a positive or negative voltage by limiting the driver current. However, this will cause large supply current and dissipation. Thermal shutdown further protects the devices from excessive temperatures that may result from a short circuit. The transmitter returns to normal operation once the short is removed.

9.4.5. Transmitter-Dominant Timeout

The CA-IF1044x family of devices features a transmitter-dominant timeout (t_{DOM}) that prevents erroneous CAN controllers from clamping the bus to a dominant level by maintaining a continuous low TXD signal. When TXD remains in the dominant state (low) for greater than t_{DOM}, the transmitter is disabled, releasing the bus to a recessive state (see Figure 9-3). After a dominant timeout fault, the transmitter is re-enabled when receiving a rising edge at TXD. The transmitter-dominant timeout limits the minimum possible data rate to 4kbps.

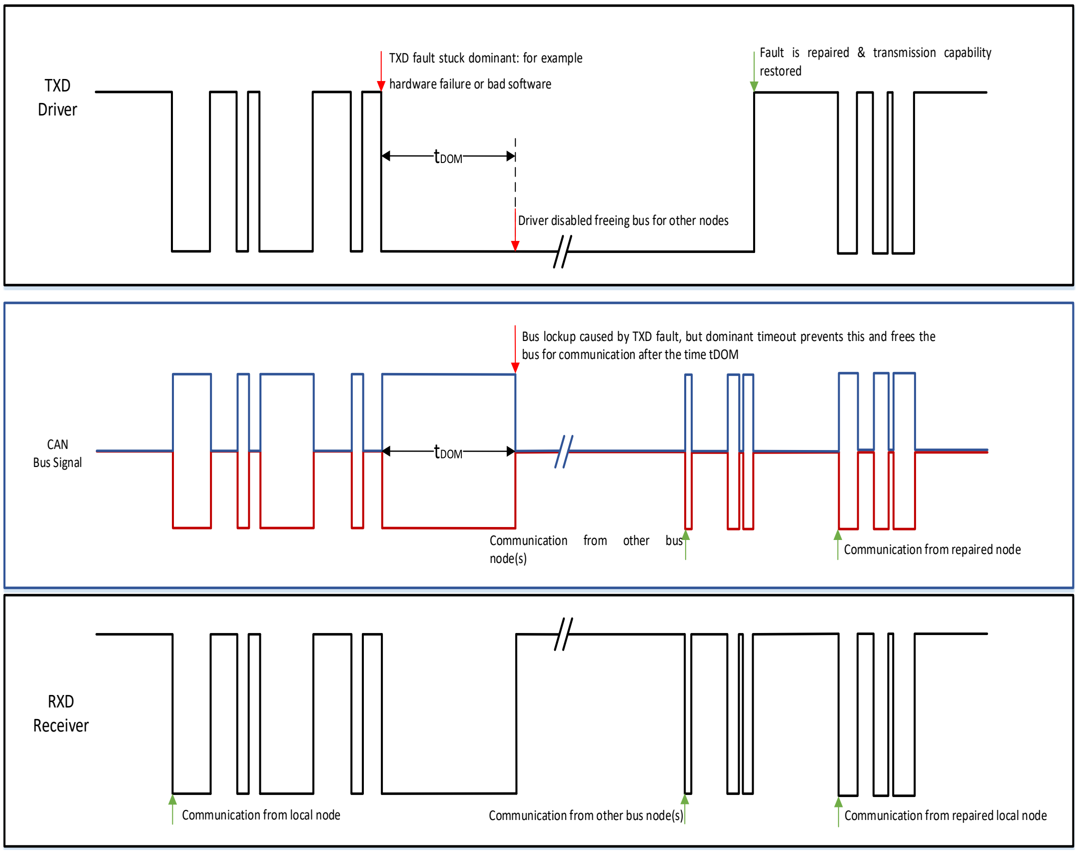


Figure 9-3. Transmitter-Dominant Timeout Protection

9.5. Unpowered Device

The device is designed to be 'ideal passive' or 'no load' to the CAN bus if it is unpowered. The bus terminals (CANH, CANL) have extremely low leakage currents when the device is unpowered to avoid loading down the bus.

9.6. Floating Terminals

These devices have internal pull-up on critical terminals to place the device into known states if the terminals float. The TXD terminal is pulled up to V_{CC} or V_{IO} to force a recessive input level if the terminal floats. The pin STB is also pulled up to force the device into standby mode if the terminal floats.

9.7. Operating Mode

All devices have two operating modes: normal mode and standby mode. Operating mode selection is made via the STB input.

9.7.1. Normal Mode

Select the normal mode of devices operation by setting STB terminal to logic-low. The CAN driver and receiver are fully operational and CAN communication is bi-directional. The driver translates a digital input on TXD to a differential output on CANH and CANL. The receiver translates the differential signal from CANH and CANL to a single-ended output on RXD.

9.7.2. Standby and Wake-up

Drive STB pin high or leave it open for standby mode, which switches the transmitter off and disables the main receiver. The low-power receive channel is enabled and put the device to a low current and low-speed monitor state. Thus the supply current is reduced during standby mode. The bus line is monitored by the low-power bus monitor, a low-speed differential comparator, to detect and recognize a wakeup event on the bus line, see Table 9-5.

Table 9-5. Operating Mode

STB	MODE	DRIVER	RECEIVER
Low	Normal	Enabled	Enabled
High or open	Standby	Disabled	Low-power receive channel is enabled and monitor the bus line.

To improve the system operation reliability and prevent false wake-up, the CA-IF1044x devices' receiver features wake-up timeout detection and filtered CAN bus status wake-up detection according to the ISO 11898-2:2016 standard. This means, for a valid dominant or recessive to be considered, the bus must be kept in that state for more than the t_{WK_FILTER} time. For a remote wake-up event to successfully occur, a dominant bus level greater than t_{WK_FILTER} must be detected and received by the low-power receive channel first to initiate a wake-up event. Then the low-power monitor will wait for a valid recessive state from CAN bus. Once a valid recessive pulse is received, the low-power bus monitor is waiting for the 2nd valid dominant state, other bus traffic does not reset the bus monitor. Once the low-power receive channel detects a successful wake-up event (a series of valid dominant - recessive - dominant pulses) within the timeout value $t \leq t_{WK\_TIMEOUT}$, RXD pulls low. CAN controller can drive the STB low based on this wake-up signal from RXD for normal operation. RXD is high until a valid wake-up is received during standby mode, see Figure 9-4 for more details.

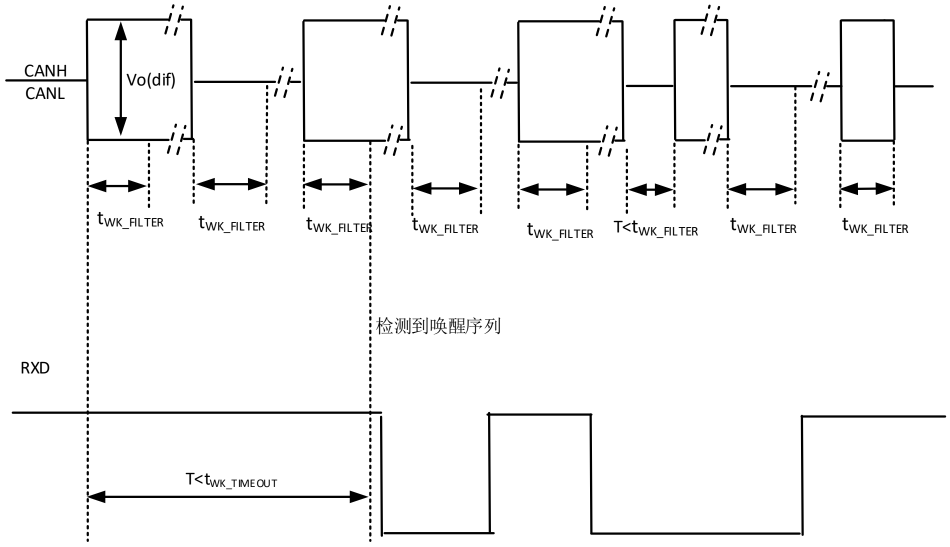


Figure 9-4. Wake-up Detection

10. Application Information

The CA-IF1044x CAN transceivers are typically used in applications with a host microprocessor or FPGA that includes the data link layer portion of the CAN protocol. Figure 10-1, Figure 10-2 show the typical application circuit for the CA-IF1044S-Q1/CA-IF1044D-Q1 and CA-IF1044Vx, respectively. In Figure 10-2, connect the V_{IO} to the MCU logic-supply.

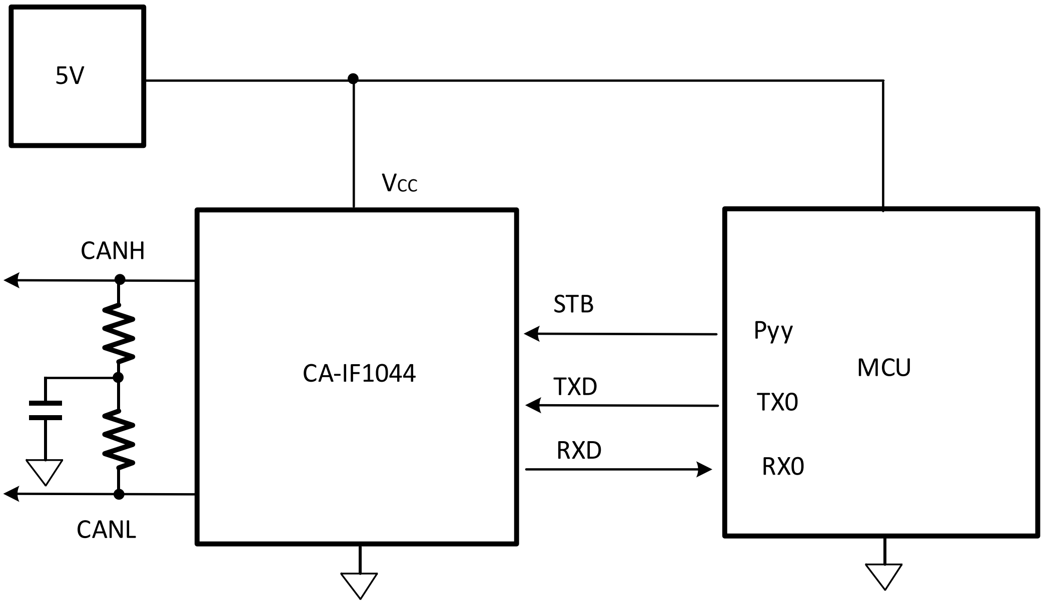


Figure 10-1. Typical Application Circuit for the CA-IF1044S-Q1/CA-IF1044D-Q1

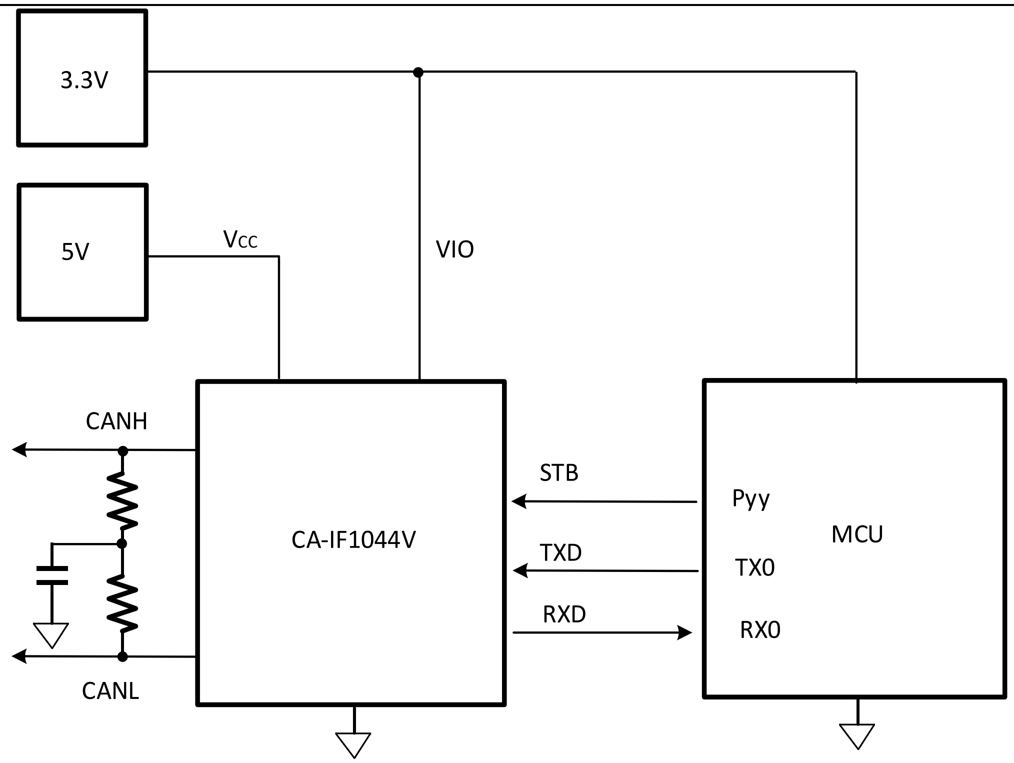
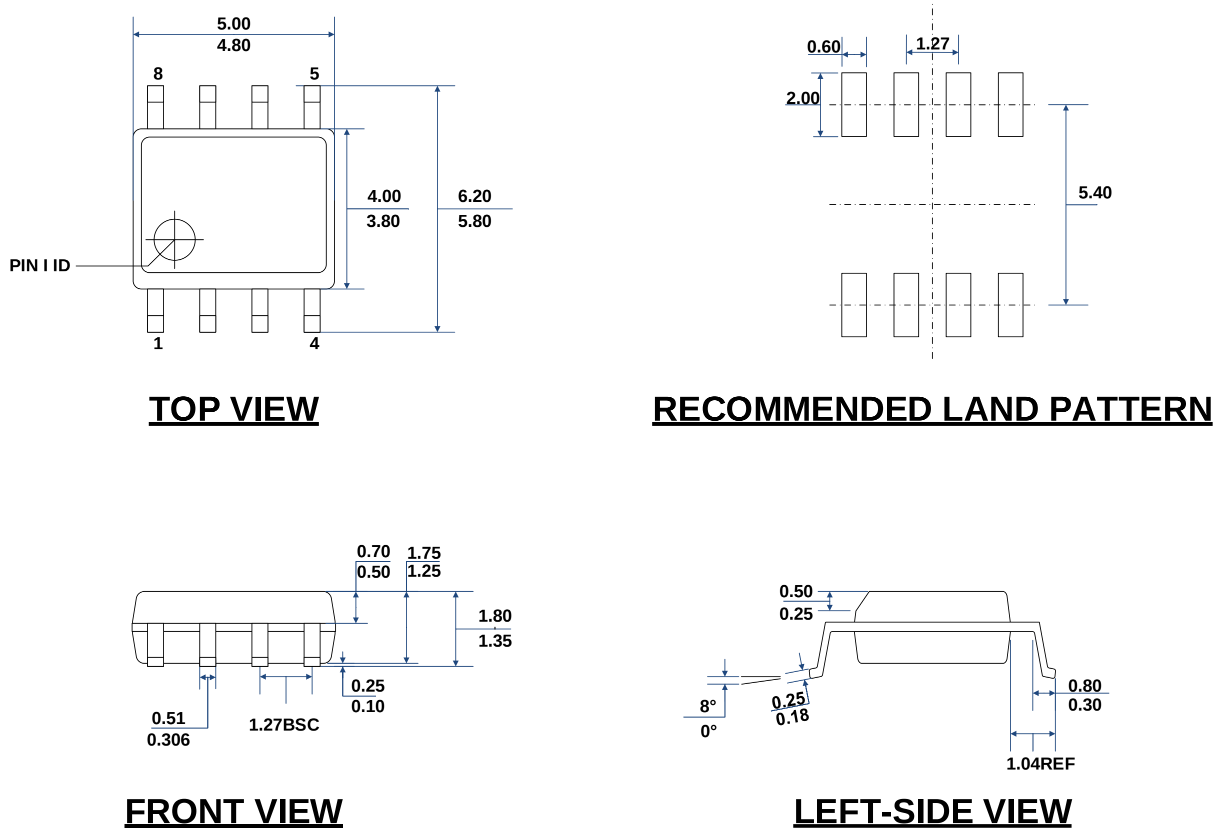


Figure 10-2. Typical Application Circuit for the CA-IF1044Vx

All of the CA-IF1044x series devices can operate up to 5Mbps data rate. However, the maximum data rate is limited by the bus loading, number of nodes, cable length etc. For CAN network design, margin must be given for signal loss across the system and cabling, parasitic loadings, timing, network imbalances, ground offsets and signal integrity thus a practical maximum data rate, number of nodes often lower. The ISO11898 Standard specifies a maximum of 30 nodes, with careful design, and consider of high input impedance of the CA-IF1044x, designers can have many more nodes on the CAN bus.

11. Package Information

SOIC8 Package Outline

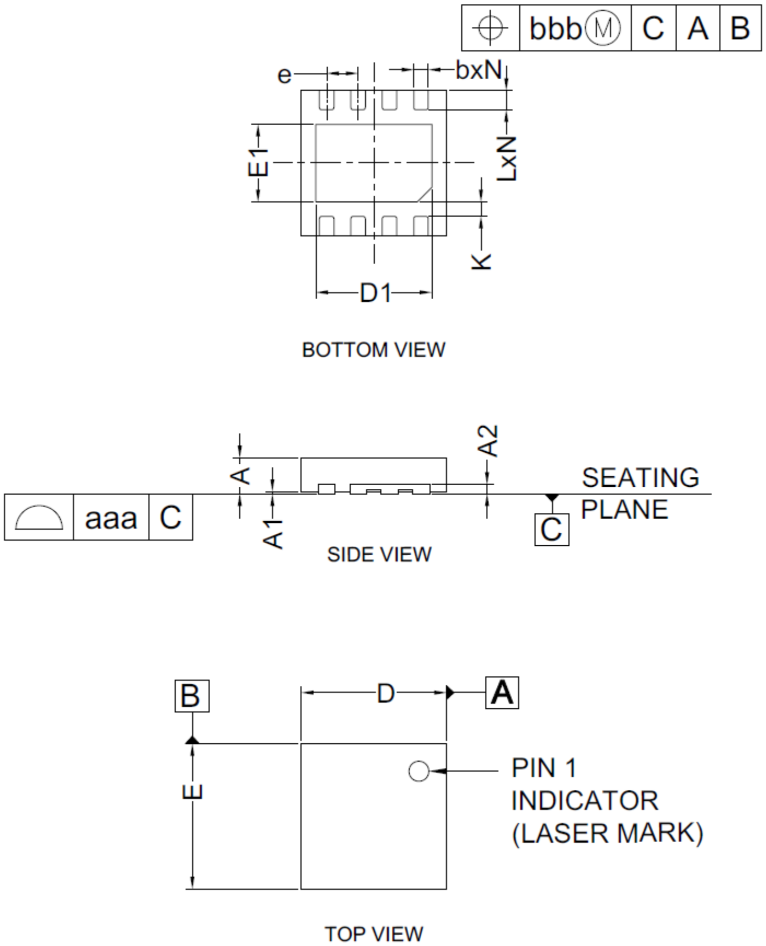


Note:

1. Controlling dimensions are in millimeters.

Figure 11-1. SOIC8 Package Outline

DFN8 Package Outline



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	TYP	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A2		0.203	
b	0.25	0.30	0.35
D	2.90	3.00	3.10
D1	2.35	2.40	2.45
E	2.90	3.00	3.10
E1	1.55	1.60	1.65
e		0.65BSC	
L	0.35	0.40	0.45
K	0.20	-	-
N		8	
aaa		0.08	
bbb		0.10	

Note:
1. Controlling dimensions are in millimeters.

Figure 11-2. DFN8 Package Outline

12. Soldering Temperature (reflow) Profile

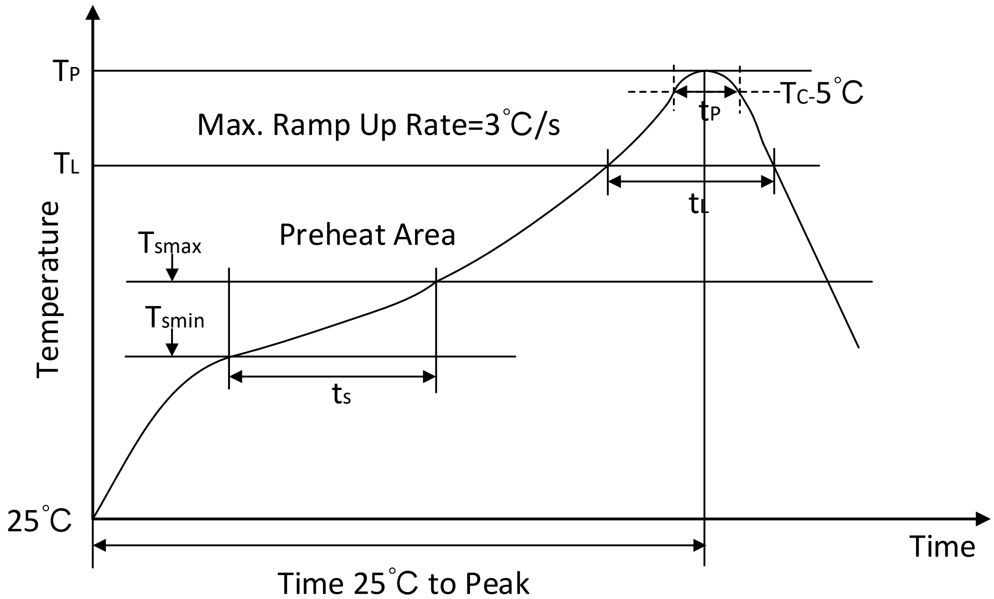


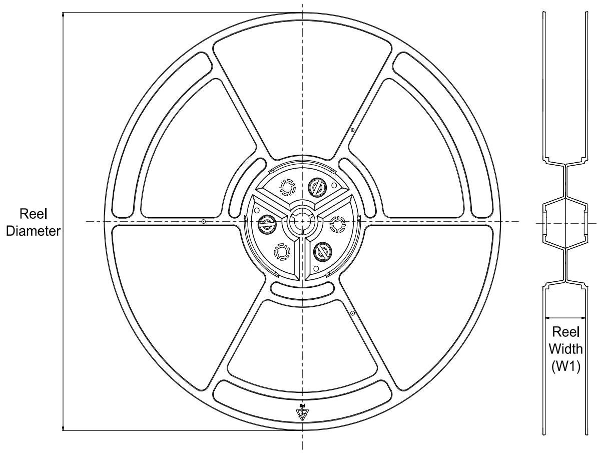
Figure 12-1. Soldering Temperature (reflow) Profile

Table 12-1. Soldering Temperature Parameter

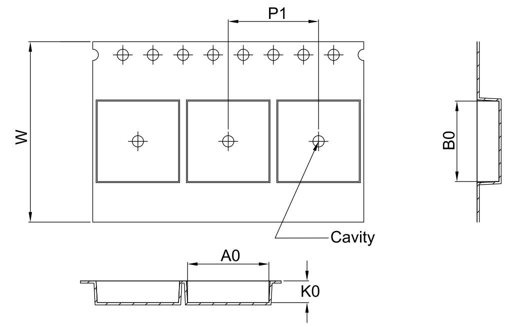
Profile Feature	**Pb-Free Assembly**
Average ramp-up rate(217 ℃ to Peak)	3℃/second max
Time of Preheat temp(from 150 ℃ to 200 ℃	60-120 second
Time to be maintained above 217 ℃	60-150 second
Peak temperature	260 +5/-0 ℃
Time within 5 ℃of actual peak temp	30 second
Ramp-down rate	6 ℃/second max.
Time from 25℃ to peak temp	8 minutes max

13. Tape and Reel Information

REEL DIMENSIONS

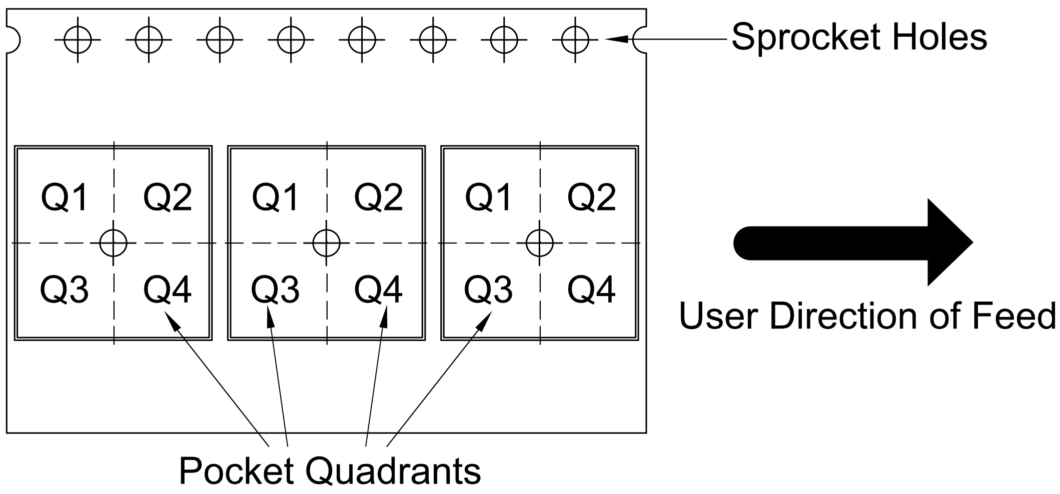


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CA-IF1044S-Q1	SOIC8	S	8	2500	330	12.4	6.40	5.40	2.10	8.00	12.00	Q1
CA-IF1044VS-Q1	SOIC8	S	8	2500	330	12.4	6.40	5.40	2.10	8.00	12.00	Q1
CA-IF1044D-Q1	DFN8	D	8	3000	330	12.4	3.35	3.35	1.13	8.00	12.00	Q1
CA-IF1044VD-Q1	DFN8	D	8	3000	330	12.4	3.35	3.35	1.13	8.00	12.00	Q1

14. Appendix

Table 14-1. Comparison Table of Parameter Symbols in SO11898-2:2016 Standard and CA-IF1044 Datasheet

ISO 11898-2:2016		**CA-IF1044 Datasheet**	
Parameter	**Note**	**Symbol**	**Parameter**
HS-PMA dominant output characteristics			
Single ended voltage on CAN_H	V_{CAN_H}	$V_{O(DOM)}$	dominant output voltage
Single ended voltage on CAN_L	V_{CAN_L}		
Differential voltage on normal bus load	V_{Diff}	$V_{OD(DOM)}$	dominant differential output voltage
Differential voltage on effective resistance during arbitration			
Optional: Differential voltage on extended bus load range			
HS-PMA driver symmetry			
Driver symmetry	V_{sym}	V_{sym}	transmitter voltage symmetry
Maximum HS-PMA driver output current			
Absolute current on CAN_H	I_{CAN_H}	$I_{OS(SS\_DOM)}$	dominant short-circuit output current
Absolute current on CAN_L	I_{CAN_L}		
HS-PMA recessive output characteristics, bus biasing active/inactive			
Single ended output voltage on CAN_H	V_{CAN_H}	$V_{O(REC)}$	recessive output voltage
Single ended output voltage on CAN_L	V_{CAN_L}		
Differential output voltage	V_{Diff}	$V_{OD(REC)}$	recessive differential output voltage
Optional HS-PMA transmit dominant timeout			
Transmit dominant timeout, long	t_{dom}	t_{DOM}	TXD dominant time-out time
Transmit dominant timeout, short			
HS-PMA static receiver input characteristics, bus biasing active/inactive			
Recessive state differential input voltage range Dominant state differential input voltage range	V_{Diff}	V_{IT}	differential receiver threshold voltage
HS-PMA receiver input resistance (matching)			
Differential internal resistance	R_{Diff}	R_{DIFF}	differential input resistance
Single ended internal resistance	R_{CAN_H} R_{CAN_L}	R_{IN}	input resistance
Matching of internal resistance	m_R	$R_{DIFF(M)}$	input resistance deviation
HS-PMA implementation loop delay requirement			
Loop delay	t_{Loop}	t_{loop2}	delay time from TXD HIGH to RXD HIGH
		t_{loop1}	delay time from TXD LOW to RXD LOW
Optional HS-PMA implementation data signal timing requirements for use with bit rates above 1 Mbit/s up to 2 Mbit/s and above 2 Mbit/s up to 5 Mbit/s			
Transmitted recessive bit width @ 2 Mbit/s / @ 5 Mbit/s, intended	$t_{Bit(Bus)}$	$t_{bit(BUS)}$	transmitted recessive bit width
Received recessive bit width @ 2 Mbit/s / @ 5 Mbit/s	$t_{Bit(RXD)}$	$t_{bit(RXD)}$	bit time on pin RXD
Receiver timing symmetry @ 2 Mbit/s / @ 5 Mbit/s	Δt_{Rec}	Δt_{Rec}	receiver timing symmetry
HS-PMA maximum ratings of V_{CAN_H}, V_{CAN_L} and V_{Diff}			
Maximum rating V_{Diff}	V_{Diff}	V(DIFF)	voltage between pin CANH and pin CANL
General maximum rating V_{CAN_H} and V_{CAN_L}	V_{CAN_H} V_{CAN_L}	V(BUS)	voltage on CANH, CANL pin
Optional: Extended maximum rating VCAN_H and VCAN_L			

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